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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,216	09/30/1998	RONALD PASQUALINI	NSC1-D8400	6392

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/164,216	PASQUALINI, RONALD	
	Examin r	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15,19 and 38-50* is/are pending in the application.

4a) Of the above claim(s) *40-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15,19,38,39 and 45-50* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 15, 19, 38-39 and 45-50 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Figure 16 depicts plurality of positive lines being connected to pads via ESD switches Claim 15 recites a plurality of second diodes connected to a pad and a positive line. There is no support for plurality of positive lines not being connected to pads, as recited in claim 15.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 15, 19, 38-39 and 40-45, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gens et al. (5,515,225) in view of Admitted Prior Art (APA).

Gens et al. teach in figure 2 a semiconductor chip having a substrate (figure 4, the external line encircling R1) of a first conductivity type, the chip comprising a plurality of pads P1, P2, an ESD negative ring R2, a plurality of ESD positive lines (the horizontal lines located between the high power supply terminals (the square blocks indicated as VDD1 and VDD2) and the line connecting the two diodes. See also column 3, lines 32-49) not being connected to a steady voltage source and not being electrically connected to each other and not encircling the periphery of the chip, a plurality of switches (diodes) connected between the ESD positive lines and the ESD negative ring, and a plurality of first and second diodes D1, D2 connected to a pad and the negative ring and positive line, respectively.

Although Gens et al. do not explicitly state that plurality of switches are connected between the ESD positive lines and the ESD negative ring, this feature is inherent in Gens et al.'s device, because it is well known in the art that diodes are switches, of which official notice is taken. Therefore, Gens et al. teach plurality of switches being connected between the ESD positive lines and the ESD negative ring, as claimed.

Gens et al. do not teach plurality of positive lines not being connected to pads.

APA teaches in figures 1 and 2 a plurality of ESD switches including a transistor (figure 2) connected to the positive line and to the negative ring, respectively (page 2, lines 24-27), wherein the plurality of positive lines not being connected to pads
It would also have been obvious to a person of ordinary skill in the art at the time the invention was made not to connect the plurality of positive lines to the pads in Gens et al.'s device in order to provide more effective unidirectional flow of current during ESD operation.

Regarding claim 19, Gens et al. teach in figure 4 a negative line encircling the periphery of the chip.

Regarding claim 39, APA teaches in figure 2 a plurality of ESD switches including a transistor. It would also have been obvious to a person of ordinary skill in the art at the time the invention was made to use a transistor as an ESD switch in Gens et al.'s device, because it is well known in the art to use a transistor as an ESD switch, of which official notice is taken.

Regarding claim 46, Gens et al. teach in figure 2 a second diode having an anode electrically connected to a pad.

Response to Arguments

5. Applicant argues on page 3 that it is improper to restrict a dependent claim, because all the limitations of the independent claim are present in the dependent claim.

The criteria for restricting dependent claims is not whether the limitations of the independent claim are present in the dependent claim. Dependent and independent claims can be restricted for being related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because diodes D1 and D2 (figure 1) can be used in the circuits of the embodiment of figure 16. The subcombination has separate utility such as diodes 800 and 1000 can be used in the circuit of figure 1. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

6. Applicant argues on page 4 that no ESD positive lines could be found in Gens et al.'s structure, and bus R1 can not be read to be a plurality of positive lines. Applicant can not determine which are the plurality of positive lines described as the horizontal

lines located between the high power supply terminals (the square blocks indicated as VDD1 and VDD2) and the line connecting the two diodes.

The examiner agrees that bus R1 can not be read to be a plurality of positive lines not electrically connected together. However, Gens et al. teach in figure 2 a plurality of ESD positive lines. Figure 2 depicts high power supply terminals as square blocks indicated as VDD1 and VDD2. Horizontal lines are connected between the right side of the square blocks (indicated as VDD1 and VDD2) and vertical lines connecting the two diodes. These horizontal lines are the positive lines in Gens et al.'s structure..

7. Applicant argues on page 4 that the leftmost D1 diode can not be read to be the second diode, because the leftmost D1 diode is connected to bus R1, and bus R1 is not a plurality of positive lines not electrically connected together.

Although bus R1 is not a plurality of positive lines not electrically connected together, bus R1 is one positive line. Therefore, the leftmost D1 diode can be one second diode connected to one pad and one positive line, whereas the rest of the D1 diodes are connected to the positive lines of VDD1 and VDD2 as described in section 6 above.

8. Applicant argues on page 5 that the horizontal lines can not be read to be the positive lines, because the plurality of the positive lines must be connected to the pads.

Applicant does not claim that the plurality of the positive lines must be connected to the pads. In fact, applicant recites in claim 15 that the plurality of the positive lines are not connected to the pads.

9. Applicant argues on pages 5 and 6 that the diodes of Gens et al. do not operate or function as switches, and thus can not be considered as switches.

Claim 15 recites ESD switches connected between the positive line and the negative switch. The broad recitation of the claim does not preclude the first or the second diode from being an ESD switch. The first and the second diode of Gens et al. conduct current in only one direction. Clearly, a diode conducting in only one direction is a switch. Therefore, either the first diode or the second diode of Gens et al. can be an ESD switch, as claimed.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in th Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722

and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday.

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

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Ori Nadav

February 5, 2002